WE CLAIM

1. Apparatus for processing data, said apparatus comprising:

data processing logic operable to perform data processing operations; and

an instruction decoder operable to decode program instructions to control said data processing logic to perform said data processing operations, wherein

said instruction decoder is responsive to a predication instruction to control said data processing logic to either execute or not execute one or more associated program instructions in dependence upon one or more condition states of said apparatus for processing data set by execution of one or more program instructions other than said predication instruction.

2. Apparatus as claimed in claim 1, wherein said predication instruction controls a plurality of associated program instructions.

3. Apparatus as claimed in claim 1, wherein said one or more associated program instructions are non-conditional program instructions.

4. Apparatus as claimed in claim 1, wherein said one or more condition states comprise values of one or more condition code flags.

5. Apparatus as claimed in claim 1, wherein said one or more condition states are evaluated at one of:

(i) once upon execution of said predication instruction; and

(ii) prior to executing each associated program instruction.

6. Apparatus as claimed in claim 1, wherein said one or more associated instructions immediately follow said predication instruction.

7. Apparatus as claimed in claim 1, wherein said predication instruction is associated with:

(i) a condition matching block of one or more program instructions to be executed if said one or more condition states match one or more predetermined conditions; and

(ii) a condition not matching block of one or more program instructions to be executed if said one or more condition states do not match said one or more predetermined conditions.

8. Apparatus as claimed in claim 7, wherein said predication instruction specifies one or more of:

(i) a length of said condition matching block of one or more program instructions; and

(ii) a length of said condition not matching block of one or more program instructions.

9. Apparatus as claimed in claim 7, wherein said predication instruction specifies said one or more predetermined conditions.

10. Apparatus as claimed in claim 1, wherein said predication instruction includes one or more fields each specifying if a respective associated program instruction is to be executed or not executed depending upon a comparison of said one or more condition states with one or more predetermined states.

11. Apparatus as claimed in claim 10, wherein said predication instruction includes a field specifying for each respective associated program instruction whether said one or more condition states or a complement of said one or more condition states is compared with said one or more predetermined states to determine if said respective associated program instruction is executed.

12. Apparatus as claimed in claim 1, comprising a program counter register operable to store an address indicative of a memory location of a program instruction being executed.

13. Apparatus as claimed in claim 1, comprising a predicated instruction counter register operable to store a counter value indicative of how many of said one or more associated program instructions subject to said predication instruction have been executed.

14. Apparatus as claimed in claim 12, wherein, when executing said one or more associated program instructions subject to said predication instruction, said program counter register continues to store an address corresponding to said predication instruction.

15. Apparatus as claimed in claim 13, comprising an exception handling circuit operable upon occurrence of an exception to store said counter value and upon completion of said exception to restart execution starting at a program instruction pointed to by said counter value.

16. Apparatus as claimed in claim 1, wherein said one or more associated instructions specify different data processing operations when subject to said predication instruction.

17. Apparatus as claimed in claim 16, wherein in dependence upon a programmable field within said predication instruction said one or more associated instructions are blocked from making any changes to said one or more condition states.

18. A method of processing data, said method comprising the steps of:

performing data processing operations with data processing logic; and

decoding program instructions with an instruction decoder to control said data processing logic to perform said data processing operations, wherein

in response to a predication instruction said instruction decoder controls said data processing logic to either execute or not execute one or more associated program instructions in dependence upon one or more condition states of said apparatus for processing data set by execution of one or more program instructions other than said predication instruction.

19. A method as claimed in claim 18, wherein said predication instruction controls a plurality of associated program instructions.

20. A method as claimed in claim 18, wherein said one or more associated program instructions are non-conditional program instructions.

21. A method as claimed in claim 18, wherein said one or more condition states comprise values of one or more condition code flags.

22. A method as claimed in claim 18, wherein said one or more condition states are evaluated at one of:
(i) once upon execution of said predication instruction; and
(ii) prior to executing each associated program instruction.

23. A method as claimed in claim 18, wherein said one or more associated instructions immediately follow said predication instruction.

24. A method as claimed in claim 18, wherein said predication instruction is associated with:

(i) a condition matching block of one or more program instructions to be executed if said one or more condition states match one or more predetermined conditions; and

(ii) a condition not matching block of one or more program instructions to be executed if said one or more condition states do not match said one or more predetermined conditions.

25. A method as claimed in claim 24, wherein said predication instruction specifies one or more of:

(i) a length of said condition matching block of one or more program instructions; and

(ii) a length of said condition not matching block of one or more program instructions.

26. A method as claimed in claim 24, wherein said predication instruction specifies said one or more predetermined conditions.

27. A method as claimed in claim 18, wherein said predication instruction includes one or more fields each specifying if a respective associated program instruction is to be executed or not executed depending upon a comparison of said one or more condition states with one or more predetermined states.

28. A method as claimed in claim 27, wherein said predication instruction includes a field specifying for each respective associated program instruction whether said one or more condition states or a complement of said one or more condition states is compared with said one or more predetermined states to determine if said respective associated program instruction is executed.

29. A method as claimed in claim 18, comprising a program counter register operable to store an address indicative of a memory location of a program instruction being executed.

30. A method as claimed in claim 18, comprising a predicated instruction counter register operable to store a counter value indicative of how many of said one or more associated program instructions subject to said predication instruction have been executed.

31. A method as claimed in claim 29, wherein, when executing said one or more associated program instructions subject to said predication instruction, said program counter register continues to store an address corresponding to said predication instruction.

32. A method as claimed in claim 30, comprising an exception handling circuit operable upon occurrence of an exception to store said counter value and upon completion of said exception to restart execution starting at a program instruction pointed to by said counter value.

33. A method as claimed in claim 18, wherein said one or more associated instructions specify different data processing operations when subject to said predication instruction.

34. A method as claimed in claim 33, wherein in dependence upon a programmable field within said predication instruction said one or more associated instructions are blocked from making any changes to said one or more condition states.

35. A computer program product comprising a computer program operable to control an apparatus for processing data having data processing logic operable to perform data processing operations and an instruction decoder operable to decode program instructions to control said data processing logic to perform said data processing operations, said computer program comprising:

a predication instruction operable to control said data processing logic to either execute or not execute one or more associated program instructions in dependence upon one or more condition states of said apparatus for processing data set by execution of one or more program instructions other than said predication instruction.

36. A computer program product as claimed in claim 35, wherein said predication instruction controls a plurality of associated program instructions.

37. A computer program product as claimed in claim 35, wherein said one or more associated program instructions are non-conditional program instructions.

38. A computer program product as claimed in claim 35, wherein said one or more condition states comprise values of one or more condition code flags.

39. A computer program product as claimed in claim 35, wherein said one or more condition states are evaluated at one of:

(i) once upon execution of said predication instruction; and

(ii) prior to executing each associated program instruction.

40. A computer program product as claimed in claim 35, wherein said one or more associated instructions immediately follow said predication instruction.

41. A computer program product as claimed in claim 35, wherein said predication instruction is associated with:

(i) a condition matching block of one or more program instructions to be executed if said one or more condition states match one or more predetermined conditions; and

(ii) a condition not matching block of one or more program instructions to be executed if said one or more condition states do not match said one or more predetermined conditions.

42. A computer program product as claimed in claim 41, wherein said predication instruction specifies one or more of:

(i) a length of said condition matching block of one or more program instructions; and

(ii) a length of said condition not matching block of one or more program instructions.

43. A computer program product as claimed in claim 41, wherein said predication instruction specifies said one or more predetermined conditions.

44. A computer program product as claimed in claim 35, wherein said predication instruction includes one or more fields each specifying if a respective associated program instruction is to be executed or not executed depending upon a comparison of said one or more condition states with one or more predetermined states.

45. A computer program product as claimed in claim 44, wherein said predication instruction includes a field specifying for each respective associated program instruction whether said one or more condition states or a complement of said one or more condition states is compared with said one or more predetermined states to determine if said respective associated program instruction is executed.

46. A computer program product as claimed in claim 35, comprising a program counter register operable to store an address indicative of a memory location of a program instruction being executed.

47. A computer program product as claimed in claim 35, comprising a predicated instruction counter register operable to store a counter value indicative of how many of said one or more associated program instructions subject to said predication instruction have been executed.

48. A computer program product as claimed in claim 46, wherein, when executing said one or more associated program instructions subject to said predication instruction, said program counter register continues to store an address corresponding to said predication instruction.

49. A computer program product as claimed in claim 47, comprising an exception handling circuit operable upon occurrence of an exception to store said counter value and upon completion of said exception to restart execution starting at a program instruction pointed to by said counter value.

50. A computer program product as claimed in claim 35, wherein said one or more associated instructions specify different data processing operations when subject to said predication instruction.

51. A computer program product as claimed in claim 50, wherein in dependence upon a programmable field within said predication instruction said one or more

associated instructions are blocked from making any changes to said one or more condition states.